REMARKS

Claims 1-10 and 12-14, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 USC § 112, Second Paragraph Rejection

Claim 2 stands rejected under 35 U.S.C. 112, second paragraph, because the Office Action argues that claim 2 is indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Office Action argues that the spacers cannot be adjacent if an etch stop layer is between them.

Claim 2 has been amended to remove the text describing that the second spacers are adjacent to the first spacers. Thus, the currently amended claim 2 defines that "said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors". Therefore, claim 2 particularly points out and distinctly claims the subject matter which Applicants regard as the invention, in compliance with 35 U.S.C. 112, second paragraph. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejection.

II. The Prior Art Rejections

Claims 1-7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kao et al. (U.S. Patent No. 6,500,765), hereinafter referred to as Kao, in view of

Krivokapic et al. (U.S. Patent No. 6,512,273), hereinafter referred to as Krivokapic. Claims 8-10 and 12-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kao and Krivokapic, and further in view of Ju (U.S. Patent No. 6,562,676), hereinafter referred to as Ju. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides an integrated circuit structure comprising first-type transistors having first spacers and second-type transistors having first spacers and second spacers. In the rejection, the Office Action argues that Krivokapic discloses a device having a double spacer, separated by an oxide layer that is used as an etch stop. In addition, the Office Action argues that Ju teaches the use of offset spacers to create source/drain extensions at optimum distances from the gate electrodes. However, neither Kao, Krivokapic, nor Ju teach or suggest an etch stop layer on the first spacer and a second spacer on the etch stop layer. Furthermore, neither Kao, Krivokapic, nor Ju disclose second silicide regions that are farther from the second-type transistors than first silicide regions are from the first-type transistors. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action argues that Krivokapic discloses a double spacer (items 20 and 33) on a p-channel device, separated by an oxide layer (38) that is used as an etch stop during the etch-back of spacer 33. In support for this contention, the Office Action cites Krivokapic, col. 5, lines 19-23, which discloses that silicon dioxide is deposited as a second liner 38. Polysilicon is subsequently deposited, and then etched back to form

polysilicon spacers 33 on n-channel and p-channel gate sidewalls (over the nitride spacers 20 for the p-channel devices). However, Krivokapic fails to teach or suggest that the second liner 38 functions as an etch stop layer. Krivokapic merely discloses that "[s]econd oxide liner 38 separates nitride and poly spacers on p-channel devices."

The Office Action asserts that it would have been obvious to combine the structures taught by Kao and Krivokapic, due to the fact that an etch stop layer allows separate materials to be chosen for spacer layers in order to optimize drive current in each type of device. In support for this argument, the Office Action cites Krivokapic, col. 6, lines 1-5, which discloses that "the spacers for p-channel and n-channel devices in a CMOS structure are separately chosen to optimize drive current in each type of device". However, the portion cited by the Office Action is completely silent as to etch stop layers. Thus, Krivokapic does not teach or suggest that an etch stop layer allows separate materials to be chosen for spacer layers.

Therefore, contrary to the position taken in the Office Action, Applicants submit that Krivokapic does not teach or suggest a double spacer on a p-channel device, separated by an etch stop layer. Accordingly, it is Applicants' position that Krivokapic does not teach or suggest the claimed feature of "first spacers ..., an etch stop layer on said first spacers, and second spacers on said etch stop layer" as defined by independent claims 1 and 8.

In addition, the Office Action argues that Ju teaches the use of offset spacers to create source/drain extensions at optimum distances from the gate electrodes. However, Ju fails to teach silicide regions proximate the spacers. Such features are defined in

independent claims 1 and 8 using the following language: "first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second-type transistors than said first silicide regions are from said first-type transistors."

As described in Applicants' abstract, before silicide formation, the etch stop film on the nitride is removed, leading to a silicide edge very close to the gates for the NFETs, which is optimum for NFETs. The double nitride spacer on the PFETs prevents the silicide from getting too close to the PFET gate, which is optimum for PFETs.

Furthermore, as described in paragraphs 0022-0023 of Applicants' disclosure, the subsequent cobalt silicide formation is limited by the distance of the final second spacer, which keeps this silicide at a distance of several hundred angstroms. The NFET has been shown to have the highest performance when the silicide is very much closer to the gate, so the double spacer technique does not produce the fastest NFET. If a single narrow spacer was used, the NFET would be optimized, but the close proximity of the silicide for the PFET, along with deep junction overrun will make a poor performance PFET. Before silicide formation, the LTO etch stop film on the nitride will be removed by HF, leading to a silicide edge very close to the gates for the NFETs while the double nitride spacer on the PFETs prevents the silicide from getting too close to the gate.

In addition, as described in paragraph 0029 of Applicants' disclosure, embodiments of the invention can selectively remove the second spacer over one type of device only. This provides a large advantage in tuning each device to bring the silicide

material closer to further from the gate depending on the best performance of that device. By using an anisotropic RIE (Reactive Ion Etch) which etches nitride selectively to oxide, the second nitride spacer can be removed by a dry etch to leave the LTO film and first spacer in place. This all dry removal process is more manufacturable than a wet etch, since it can be controlled to etch at a slower rate and it is not isotropic, as wet etches are.

Therefore, unlike the claimed invention, Ju fails to teach or suggest the use of silicide regions. Moreover, Ju does not disclose second silicide regions that are farther from the second-type transistors than first silicide regions are from the first-type transistors. Thus, it is Applicants' position that Ju does not teach or suggest the claimed feature of "first silicide regions proximate said first spacers of said first-type transistors; and second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors" as defined by independent claims 1, and 8.

Furthermore, Applicants respectfully submit that Ju teaches a device wherein both transistors have double spacers, while the claimed invention provides a structure wherein only the second-type transistors include second spacers. As noted above, as described in paragraph 0029 of Applicants' disclosure, embodiments of the invention can selectively remove the second spacer over one type of device only. This provides a large advantage in tuning each device to bring the silicide material closer to further from the gate depending on the best performance of that device. As also noted above, as described in paragraphs 0022-0023 of Applicants' disclosure, before silicide formation, the LTO etch

stop film on the nitride will be removed by HF, leading to a silicide edge very close to the gates for the NFETs while the double nitride spacer on the PFETs prevents the silicide from getting too close to the gate.

Therefore, Applicants submit that Ju does not teach or suggest a structure wherein only the second-type transistors include second spacers. Thus, it is Applicants' position that Ju does not teach or suggest the claimed feature wherein "said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors" as defined by dependent claim 2; or, wherein "said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors" as defined by dependent claim 9.

Therefore, it is Applicants' position that the proposed combination of Kao, Krivokapic, and/or Ju does not teach or suggest many features defined by independent claims 1 and 8; and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-10, and 12-14 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-10 and 12-14, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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